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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/042,264	01/11/2002	Satoshi Inaba	P 284163 01F181	6258

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EXAMINER
DICKEY, THOMAS L

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 07/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/042,264	INABA, SATOSHI	
	Examiner	Art Unit	
	Thomas L Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 April 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-46* is/are pending in the application.

4a) Of the above claim(s) *12-46* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 9-11* is/are rejected.

7)☒ Claim(s) *6-8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The amendment filed on 04/25/03 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1,4,5, and 11 stand rejected under 35 U.S.C. 102(a) as being anticipated by KAWASHIMA (6,163,053).

Kawashima discloses a semiconductor device with a semiconductor substrate having a surface, a gate electrode 13 formed of a poly-silicon film over the surface of the semiconductor substrate with a gate dielectric 18 interposed therebetween, a pair of source and drain diffusion layers, each having a low resistivity region 152,154 and an extension region 194 being formed to extend from this low resistivity region 152,154 toward the channel region and being lower in impurity concentration and shallower in depth than the low resistivity region 152,154, formed in the semiconductor substrate to oppose each other with a channel region laterally residing therebetween at a location immediately beneath the gate electrode 13, a first impurity doped layer 19 of a first conductivity type formed in the channel region between the source/drain diffusion layers

152/154/194, a second impurity doped layer 156 of a second conductivity type selectively formed in a region immediately beneath the gate electrode 13, under the first impurity doped layer 19; and a third impurity doped layer 15 of the first conductivity type formed under the second impurity doped layer 156, wherein the three impurity doped layers 19,156, and 15 make up a multilayer lamination structure with two junctions, wherein each of the first and second impurity doped layers 156 is formed in a layer on the semiconductor substrate with the third impurity doped layer 15 formed therein, wherein the first impurity doped layer 19 is equal to or less in junction depth than the extension region 194 of each of the source/drain diffusion layers (note that the first impurity doped layer is shown without a part # in figure 8c, and described as "another implantation ... channel regions" without a part # in column 7 lines 48-50 and 56-58) and the second impurity doped layer 156 is determined in impurity concentration and thickness to ensure that this layer is fully depleted (note column 2 lines 20-24) due to a built-in potential creatable between the first 19 and third 15 impurity doped layers. Note figures 5 through 8c, column 2 lines 20-24, column 7 lines 16-67, and column 8 lines 1-37 of Kawashima. Note especially column 8 lines 10-13, describing low impurity concentration extension region 194, and column 8 lines 29-33, describing low resistivity regions 152 and 154.

The applicant's claim 4 does not distinguish over the Kawashima reference regardless of the process used to form the first and second impurity doped layers,

because only the final product is relevant, not the recited process of forming said layers into an undoped semiconductor layer as has been epitaxially grown.

Note that a "product by process" claim is directed to the product per se, no matter how actually made. In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear. See also MPEP 706.03(e).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

A. Claims 2 and 3 stand rejected under 35 U.S.C. 103(a) as being unpatentable over KAWASHIMA (6,163,053).

Kawashima discloses a semiconductor device with all the limitations of claims 2 and 3 except that the first impurity layer (the layer in which the channel is formed) is either partially or fully depleted. Note figures 5 through 8c, column 2 lines 20-24, column 7 lines 16-67, and column 8 lines 1-37 of Kawashima. It is noted that if the first impurity region is neither partially nor fully depleted, no channel can form, and the device will not function. Although Kawashima's device does not teach the exact types of depletion as that claimed by Applicant, the depletion differences are considered obvious design choices and are not patentable unless unobvious or unexpected results are obtained from these changes. It appears that these changes produce no functional differences and therefore would have been obvious. Note *In re* Leshin, 125 USPQ 416.

B. Claims 9 and 10 stand rejected under 35 U.S.C. 103(a) as being unpatentable over KAWASHIMA (6,163,053) in view of CHEEK ET AL. (6,162,694).

Kawashima discloses a semiconductor device with all the limitations of claims 9 and 10 except that the gate electrode is formed of a metal film as contacted with the gate electrode film. Note figures 5 through 8c, column 2 lines 20-24, column 7 lines 16-67, and column 8 lines 1-37 of Kawashima.

However, Cheek et al. discloses a method for replacing polysilicon gate electrodes with metal gate electrodes. Note figure 1 of Cheek et al. Therefore, it would have been obvious to a person having skill in the art to replace the polysilicon gate electrodes of Kawashima's semiconductor device with the metal gate electrodes such as taught by

Cheek et al. in order to reduce the conductivity and increase the electric field of the gate electrodes to thus provide a more compact, faster semiconductor device.

Allowable Subject Matter

4. Claims 6-8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

5. Applicant's arguments filed 04/25/03 have been fully considered but they are not persuasive.

At page 3 of the remarks it is argued, "Kawashima does not disclose that the three regions, 15,19, and 156, make up a multilayer laminate structure with two junctions therebetween." However, in his remarks, applicant does not indicate which features of a "multilayer laminate structure" are missing from the art. Applicant's original specification refers to a "multilayer laminate structure" in only a single place. At page 10 lines 10-17, describing the first embodiment of figure 1, applicant states that

> A silicon substrate 1 has its top surface in which a p-type impurity doped layer 2 is formed by well ion implantation techniques. Formed on this p-type layer 2 are a lightly-doped n (n^-) type impurity doped layer 3 of low impurity concentration and further a p-type impurity doped layer 4 for use as a channel region. These layers 2-4 make up a multilayer lamination structure with $p/n^-/p$ junction.

There is nothing in this description that requires the second layer to cover the third layer completely, as it does in applicant's exemplary figure 1 embodiment, rather than

partially, as it does in Kawashima. Further, it is not proper to read limitations appearing in the specification into a claim when these limitations are not recited in the claim. See *In re Paulsen*, 30 F.3d 1475, 1480, 31 USPQ2d 1671, 1674 (Fed.Cir. 1994) *Intervet America Inc. v. Kee-Vet Lab. Inc.,* 887 F.3d 1050, 1053, 12 USPQ2d 1474, 1476 (Fed.Cir. 1989). Surely Applicant would not argue that a "multilayer laminate structure" requires that the second layer be lightly doped n type, merely because the second layer of the exemplary embodiment is lightly doped n type?

Further, to allow the limitation of a "multilayer laminate structure" to eliminate structures, such as Kawashima's, where the second layer only partially covers the third would be inconsistent with the claims taken as a whole. Note that claim 5, which depends from claim 1, requires that the second layer be "selectively formed in a region immediately beneath said gate electrode."

Conclusion

6. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 703-308-0980. The examiner can normally be reached on Monday through Thursday 8 AM to 6 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 306-3431.

tld
06/2003

Minhloan Tran
Primary Examiner
Art Unit 2826